

CLAIMS

What is claimed is:

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1. A method comprising:
 - 2 providing a first taken/not-taken prediction responsive to an address using a
 - 3 saturating counter branch predictor;
 - 4 providing (1) a second taken/not-taken prediction responsive to the address
 - 5 resulting in a hit in a local branch history table, and (2) a hit/miss indication for the
 - 6 address; and
 - 7 selecting for the address one of (1) the second prediction if the indication is a hit,
 - 8 and (2) the first prediction if the indication is a miss.
 2. The method of claim 1 further comprising:
 - 2 hashing the address prior to indexing at least one of the saturating counter
 - 3 branch predictor and the local branch history table.
 3. The method of claim 1 further comprising:
 - 5 updating a replacement field for a matching entry in the local branch history
 - 6 table only if the first prediction is incorrect, indicating that the entry is used to make a
 - 7 prediction.
 4. The method of claim 1 further comprising:
 - 2 fetching at least one instruction at the address; and
 - 3 decoding the at least one instruction, wherein at least one of the first and second
 - 4 predictions is available when the at least one instruction is being decoded.

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1 5. The method of claim 4 wherein the at least one instruction is a branch, the
2 method further comprising:
3 determining a target address of the branch; and
4 loading an IP generator with the target address if at least one of the first and
5 second predictions indicates that the branch is to be taken.

1 6. A processor comprising:
2 an instruction pointer (IP) generator capable of providing an address;
3 saturating counter branch prediction (SCBP) logic having an input coupled to the
4 IP generator and capable of providing a first taken/not-taken prediction at an output
5 responsive to the address;
6 local branch history prediction (LBHP) logic having an input coupled to the IP
7 generator and capable of providing (1) a second taken/not-taken prediction at an
8 output responsive to the address resulting in a hit, and (2) a hit/miss indication for the
9 address; and
10 a multiplexer having an input coupled to the outputs of the SCBP and LBHP
11 logic and a select input coupled to receive the hit/miss indication and in response
12 provide (1) the second prediction if there is a hit and (2) the first prediction if there is a
13 miss.

1 7. The processor of claim 6 further comprising:
2 address hash logic coupled between the IP generator and the inputs of the SCBP
3 and LBHP logic to provide a plurality of index values to at least one of the SCBP and
4 LBHP logic.

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1 8. The processor of claim 6 wherein the SCBP logic includes a bimodal
2 predictor.

1 9. The processor of claim 6 wherein the LBHP logic includes a plurality of
2 local branch history tables each to provide a tag and a taken/not-taken history
3 associated with the tag in response to a hit, compare logic coupled to each of the
4 plurality of tables to determine the hit/miss indication, history multiplexer coupled to
5 each of the plurality of tables to provide the history for the hit, and combinational logic
6 coupled to an output of the history multiplexer to provide the second taken/not-taken
7 prediction.

1 10. The processor of claim 6 wherein the LBHP logic includes at least one
2 local branch history table to provide a tag and a taken/not-taken history in response to
3 a hit, the processor further comprising:
4 entry replacement logic to update a replacement field for a matching entry
5 in the at least one table only if the first prediction is incorrect.

1 11. The processor of claim 6 further comprising:
2 an instruction fetch stage of a pipeline; and
3 an instruction decode stage of the pipeline, and wherein the prediction at the
4 output of the multiplexer is available when the address is being processed by an
5 instruction decode stage of a pipeline.

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1 12. The processor of claim 11 wherein the decode stage is capable of
2 determining a target address of a branch instruction located at the address, the
3 processor further comprising
4 control logic coupled to load the IP generator with the branch target address if an
5 output of the multiplexer indicates, for the address, that a branch is predicted to be
6 taken.

1 13. The processor of claim 6 wherein the address points to a cache line having
2 a plurality of instructions.

1 14. An apparatus comprising:
2 means for providing an address of at least one instruction;
3 means for providing a first taken/not-taken branch prediction based upon the
4 current state of a state machine and responsive to the address;
5 local branch history prediction (LBHP) logic having an input coupled to the
6 address providing means and capable of providing (1) a second taken/not-taken
7 prediction at an output responsive to the address resulting in a hit, and (2) a hit/miss
8 indication for the address; and
9 a multiplexer having an input coupled to the outputs of the first prediction
10 means and the LBHP logic and a select input coupled to receive the hit/miss indication
11 and in response provide (1) the second prediction if there is a hit and (2) the first
12 prediction if there is a miss.

1 15. The apparatus of claim 14 further comprising:

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2 means for encoding the address to provide a plurality of index values to at least
3 one of the first prediction means and the LBHP logic.

1 16. The apparatus of claim 14 wherein the LBHP logic includes a plurality of
2 local branch history prediction tables each to provide a tag and a taken/not-taken
3 history associated with the tag in response to a hit, compare logic coupled to each of the
4 plurality of tables to determine the hit/miss indication, history multiplexer coupled to
5 each of the plurality of tables to provide the history for the hit, and combinational logic
6 coupled to an output of the history multiplexer to provide the second taken/not-taken
7 prediction.

1 17. The apparatus of claim 14 wherein the LBHP logic includes at least one
2 local branch history prediction table to provide a tag and a taken/not-taken history in
3 response to a hit, the processor further comprising:

4 means for updating a replacement field for a matching entry in the at least one
5 table only if the first prediction is incorrect.

1 18. The apparatus of claim 14 further comprising:
2 means for fetching at least one instruction at the address; and
3 means for decoding the at least one instruction, wherein at least one of the first
4 and second predictions is available when the at least one instruction is being decoded.

1 19. The apparatus of claim 18 wherein the at least one instruction is a branch,
2 the apparatus further comprising:

3 means for determining a target address of the branch; and

